L Number	Hits	Search Text	DB	Time stamp
-	1	("5,854,513").PN.	USPAT; US-PGPUB	2003/12/05 14:06
-	2935	(257/737,774,781).CCLS.	USPAT; US-PGPUB	2003/12/05 14:22
-	402	((257/737,774,781).CCLS.) and @pd>20030408	USPAT; US-PGPUB	2003/12/05 14:22

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 6617655 B1	22	MOSFET device with multiple gate contacts offset from gate contact area and over source area	257/401	257/737; 257/738; 257/759; 257/762; 257/766	Estacio, Maria Cristina B. et al.
2	US 6613662 B2	19	Method for making projected contact structures for engaging bumped semiconductor devices	438/613	257/678; 257/687; 257/737; 257/738; 257/778; 257/780; 257/E21.511; 257/E23.021; 257/E23.068; 438/106; 438/108; 438/25; 438/51; 438/578; 438/64	Wark, James M. et al.
3	US 6590297 B2	11	Semiconductor chip having pads with plural junctions for different assembly methods	257/786	257/203; 257/207; 257/208; 257/691; 257/693; 257/737; 257/774; 257/783; 257/784; 257/788; 257/E23.02; 257/E23.021; 29/840; 324/755; 438/614; 438/754	Sasaki, Masao
4	US 6580173 B2	12	Semiconductor device and manufacturing method of semiconductor device	257/774	257/783; 257/E21.503; 257/E21.505; 257/E23.004	Okada, Akira et al.

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
5	US 6577017 B1	8	Bond pad having vias usable with antifuse process technology	257/786	257/734; 257/750; 257/763; 257/764; 257/765; 257/774; 257/780; 257/E23.02	Wong, Richard J.
6	US 6559544 B1	6	Programmable interconnect for semiconductor devices	257/758	257/750; 257/774; 257/776	Roth, Alan et al.
7	US 20030080421 A1	14	Semiconductor device, its manufacturing process, and its inspecting method	257/737		Sawai, Keiichi et al.